RADIATION-INDUCED CLOCK JITTER AND RACE

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ABSTRACT

This study assesses the reliability risk due to radiation-induced single event upsets (SEU) of clock nodes for flip flop and pulse latch based designs. Two basic upset modes are identified: radiation-induced clock jitter and radiation-induced race. Our simulation results indicate that the radiation-induced clock soft error rate (SER) cannot be neglected on the chip-level. Particularly for pulse latch based designs, upsets occurring in the clock generator have the potential to dominate the chip-level SER if no mitigation techniques are applied. Our results show that the hardened pulse latch in combination with a hardened and shared pulse generator yields a 20x improvement in sequential SER as well as the lowest susceptibility to radiation-induced race and clock jitter with little area and performance penalty. [*Keywords:* SEU, SER, jitter, race, clock, logic, radiation, soft error rate, single event effects, sequential, alpha-particles, neutrons]

INTRODUCTION

It is well known since the 1970s that ionizing radiation, such as alpha particles and neutrons, can result in so called soft errors (SE) in memory arrays. However, the radiation-induced soft error rate (SER) of modern microprocessors, whose caches and large memory arrays are protected by parity or error checking and correction codes (ECC), is dominated by the failure rate of sequentials such as flip flops (FF) and latches [1, 2]. Whereas the SER of sequentials has been studied extensively, failure rates due to upsets in clock buffers that result in glitches propagating along the clock path and in incorrectly latched data have not been addressed yet in detail. Initial work on radiation-induced clock jitter has been reported by our group in a recent paper [3], but this study did not address the chip-level perspective and radiation-induced race.

In this contribution we are reporting on the SER risk due to upsets occurring along the global and local clock paths. A modern microprocessor clock grid requires a huge RLC network. Using SPICE to model this type of network can take an impractically long time. We therefore are introducing a methodology for assessing the SER risk of the global part of the clock path that gives sufficiently accurate results and is independent of SPICE based algorithms, as the one introduced in [3].

Figure 1 depicts the schematic representation of a typical clock distribution topology of a modern microprocessor. After the clock signal (GCLK) is synthesized in the phase-locked loop PLL (not shown in Figure 1), the signal is distributed across the die. Regional clock distribution of the clock studied here was achieved via a clock grid ("Clock Grid" in Figure 1) that was implemented in a high-level interconnect metal layer. The local distribution of the clock signals from the grid either feed into receivers directly or are locally buffered. The studied design included clock control registers that are typically used for modifying or testing the clock signal. Clock buffers and nodes internal to the clocked elements were accounted for in our analysis too, but in those cases a SPICE based simulation methodology was applied ([3]; see next section for more details).

The goal of this study is to quantify the SER risk due to radiation-induced single event upsets (SEU) along the clock path on the chip-level. We summarize all upset modes that occur due to strikes on clock nodes under the term radiation-induced clock upsets. In particular, the reliability risk due to radiation-induced clock upsets is assessed for two very different sequential designs, a master-slave type flip flop (M/S FF) and a pulse latch (PL) based design.

In the remainder of this paper we will simplify our naming convention and frequently drop the term "radiation-induced".

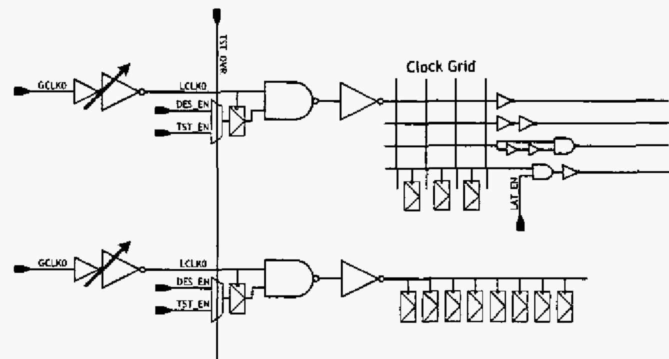

FIGURE 1. CLOCK DISTRIBUTION TOPOLOGY

In principle one can distinguish two modes of clock node upsets. Figure 2 schematically depicts the impact of both upset modes on the timing of data propagating along a data path. IN and OUT are the input and output nodes of the pipeline stage, CLK denotes the external clock node and SN the data path node just before the receiving sequential (a FF in this case).

A) Radiation-induced clock jitter: Clock jitter is defined as the difference in clock arrival times at the same sequential. Charge injected into clock nodes by ionizing radiation at times that are very close to when the clock is asserted results in the clock edge moving randomly in time. In this case a setup time (Ts) violation might occur, i.e., the clock edge is shifted such that for critical paths, data will not be latched correctly. Data arrive too late at the receiving latching element (Figure 2 – Jitter case). Please note that both NMOS and PMOS hits can result in an early rising clock edge in Figure 2, depending on the number of logic inversions between the upset node and the receiving clock node in the sequential.

B) Radiation-induced race: This mode reflects a false opening of the receiving sequential and data racing through it. For a

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short data path and without any irradiative effects data would sit at the input of the receiving sequential until the clock asserts (Figure 2: at node SN data arrive early – Race case). However, due to a particle strike enough charge might be injected to result in the formation of a new clock pulse (Figure 2). If the width of the pulse is wide enough, this could result in a false opening of the sequential and in data racing through two consecutive pipeline stages instead of one. In design this phenomenon is called race and hence the naming convention. In Figure 2 the additional clock pulse results in a premature latching of the input data (see timing diagram of node OUT in the case of race). Please note that for a long data path where the data arrive at the receiving sequential after the generation of the clock pulse, no upset occurs. This is because only the old data (i.e.., data from the previous cycle) are propagating through the sequential. It is worth mentioning that the corrupted data might not make it to the next sequential in time (i.e., sequential after OUT in Figure 2) and might be overwritten later by the correct data. However, in this study we assume that the wrong data will always win the race which results in a conservative estimate of the failure rate. Please note that race here is slightly different from classical min delay, where a new clock edge is not formed, but local clock skew results in a hold time violation. Although radiation-induced min delay upsets are possible, they are neglected here, since design margins are usually sufficient to guard against this radiation-induced race mode.

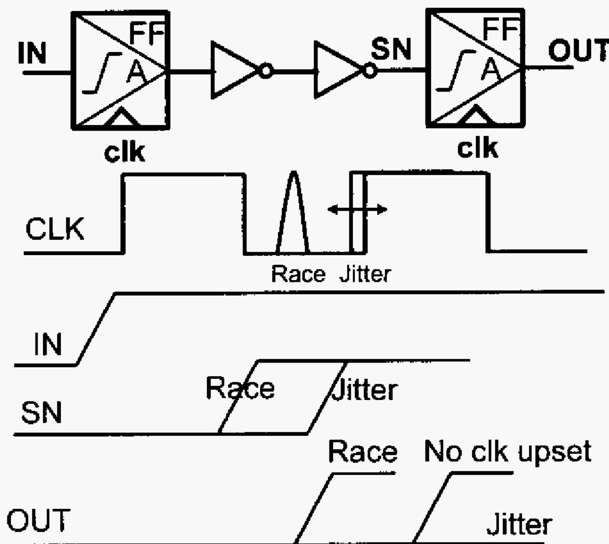

FIGURE 2. RADIATION-INDUCED JITTER AND RACE

SIMULATION APPROACH

In this study clock nodes are divided up into clock nodes that are part of the sequential library element ("internal") and clock nodes that are external to that ("external" clock nodes). Two different SER assessment approaches are applied to internal and external nodes.

External Clock Nodes – Analytical Approach

SER of clock nodes that are *external* to the library elements is assessed in a 3-step process:

a) The propagation of pulses is modeled for the technology under investigation as a function of pulse width and gate delay and distance to the receiver.

b) The critical pulse width (Wcrit) and the window of vulnerability (Twov) of the receivers (sequentials and pre-charged logic) that results in the latching of incorrect data is simulated for calibration purposes.

c) Wcrit is propagated according to a) and the SER that corresponds to the propagated pulse width at the node of interest is computed using a 1-gate SPICE simulation.

The technology calibration needs to be conducted only once for a specific technology and product. To assess the chip-level SER due to clock upsets of all clock nodes that are external to the receivers, steps b) and c) are repeated until all paths have been covered. The algorithm used is described in more detail in the next section. The objective was to estimate the SER within a factor of two with respect to accurate SPICE simulations that have been conducted for testing purposes on a few clock path sections.

Internal Clock Nodes – Fully SPICE based SER Simulations

In this approach the SER contribution of clock nodes that are internal to the clocked receivers are simulated accurately using SPICE simulations as described in great detail in [3]. We call this approach and tool TIDEST (TIme DEpendent Soft Error Tool).

Typically, the soft error rate of a circuit is assessed under static conditions, assuming that all the inputs and outputs are driven by a constant voltage. This simulation procedure is well suited for calibration and assessment purposes of the SER of memory cells and latch arrays, since the SER of memory cells and latches are measured quasi statically and the failure rates can be characterized by a constant critical charges Qcrit. Please note that Qcrit is defined as the minimum charge that results in an upset [3]. The actual SER of devices placed on a real microprocessor can be very different from the data collected under static conditions, since the inputs typically vary as a function of time, resulting in dynamic biasing conditions.

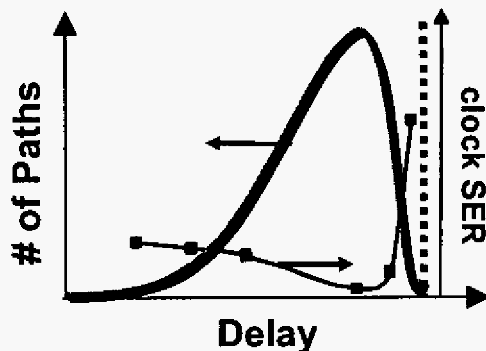

FIGURE 3. CHIP-LEVEL CLOCK NODE UPSET CONTRIBUTION IS COMPUTED BY INTEGRATING THE CLOCK SER AS A FUNCTION OF DELAY OVER THE PATH DELAY DISTRIBUTION.

The simulation procedure to assess the SER of a circuit element under realistic conditions is explained in detail in [3, 4]. In this methodology, charge is injected into clock nodes of interest and the output of the receiver (i.e. FF or pulse latch) is monitored. Qcrit together with the collection area determines the SER. The waveforms that mimic the charge collection dynamics have been calibrated

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based on a combination of experimental and device simulation data for neutrons and alpha particles. In the case of internal clock nodes, the SER is simulated and parameterized as a function of the data arrival time for all frequently used sequentials.

The final chip level SER due to upsets occurring in (internal or external) clock nodes is ideally computed by integrating the SER as a function of data arrival time over the complete path delay distribution (see Figure 3). Such a complete path delay distribution is difficult to get for the whole chip. In this study, we therefore determined the tail of the distribution of critical paths accurately and approximated the rest of the distribution using a total number of paths estimate and a best guess shape factor determined from the path delay distributions of several chip sections.

ANALYTICAL CLOCK-SER MODELING ALGORITHM

Wcrit calibration and modeling

The modeling and calibration of Wcrit is divided into two steps: determining the Wcrit at the clock input of the sequential and its propagation along the clock path. A schematic representation of the simulation setup for computing Wcrit and Twov at the receiver is depicted in Figure 4 at the example of a flip flop based path. Pulses of variable width are injected into the clock input of the receiver at different times for a constant data arrival time. The minimum pulse width that results in an upset is called Wcrit. The time period during which pulses of width Wcrit result in upsets defines Twov. This procedure is repeated for several different data arrival times, or more accurately timing margins. Margin here denotes the difference between data and clock arrival times at a sequential element.

Our study shows that for Ts violations (i.e., clock jitter), Wcrit is a strong function of the data arrival time. For race violations, however, Wcrit and consequently Qcrit are fairly constant as will be shown in the results and discussion section. This can be easily understood by noting that for jitter the clock edge is only moved. The charge or equivalently pulse width to move the clock edge sufficiently to result in a Ts violation depends on the data arrival time.

Generating a new clock edge, as it is the case for race, requires larger/wider pulses and more charge. However, the pulse width involved in race is independent of the data arrival time. Generating a new clock edge requires always the same amount of charge at the given use conditions (i.e., Vcc etc).

$Wcrit^n$ denotes the minimum width of the pulse at distance n from the receiver that after propagation to the internal clock nodes of the receiver yields a pulse of width Wcrit. We have developed an analytical model for Wcrit propagation along the clock paths. This model is based on the electrical characteristics of gates. Please note that Wcrit propagation is in principle the same as the propagation of a voltage pulse along a static combinational network. In fact, the modeling was performed by studying the propagation and shape of pulses along static gates. Our model is an improved version of the model introduced in [5]. The input to the model is the Wcrit required at the receiver and the gate delays of each device along the path. The model then computes $Wcrit^n$ at the gates of interest. The model starts calculating Wcrit from the receiver and propagates Wcrit upstream along the clock path, i.e. the pulse width required at every node along the clock path is computed.

The algorithm described above gives pulse width estimates (full width half maximum) that are within 2% of accurate SPICE simulations. Please note that our algorithm assumes rail to rail pulses.

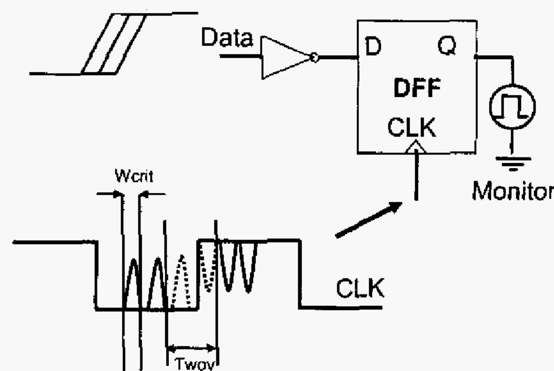

FIGURE 4. CALIBRATION METHODOLOGY FOR DEFINING WCRIT AND TWOV

Timing Derating (TD) of radiation-induced clock jitter:

As mentioned in the introduction, we have to differentiate between clock jitter and race. The former shifts the original clock edge, whereas the latter results in the formation of an additional clock edge or pulse. We will first discuss the timing derating for jitter. We have conducted extensive TIDEST simulations to assess the TD factors as a function of data arrival time.

The setup time, Ts, of a sequential denotes the time period during which the data is stable before the latching edge of the clock. Any disturbance along the clock path which results in a violation of Ts potentially causes erroneous information to be latched i.e., prevents new data from being latched. Jitter shifts the latching edge of the clock and a fault is latched if the clock input of the sequential is not stable due to a particle strike on the clock network for a time period of Ts after the data arrive. In the case of radiation-induced jitter the edge is only shifted and no clock pulse (i.e., 2 edges) is formed. Therefore, the difference between the glitch arrival time and the time the clock signal asserts is less or equal Wcrit, i.e. the width of the radiation-induced glitch. The timing window during which a particle strike can result in a soft error is denoted by Twov_jitter. Twov_jitter is function of pulse width, Wcrit, the clock signal and data arrival times, Tca and Tda, and can be approximated by

$$\text{Twov_jitter} \sim \text{Wcrit} + 2*\text{Ts} - (\text{Tca} - \text{Tda}) \qquad (1)$$

According to equation (1) Twov_jitter decreases with increasing margin (i.e., Tca-Tda). In the worst case Twov ~ Wcrit + Ts when data arrive on the critical path assuming no margin, i.e. Tca – Tda ≈ Ts. In this case a glitch on the clock path reduces the time between Tda and Tca to a value less than Ts. Please note that worst case Twov reflects the largest possible value for Twov_jitter. Jitter doesn't occur if data arrive at the receiver earlier than the worst case Twov.

The critical pulse width for race, in contrast to jitter, is fairly independent of the data arrival time. Twov due to radiation-induced race can be approximated using

$$\text{Twov_race} \sim \text{Tca} - (\text{Tda}+\text{Twov_jitter}) \qquad (2)$$

Equation (2) simply denotes the time interval between the data arrival time and the onset of jitter.

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The corresponding timing derating factors, TD, equal the ratio of Twov and the cycle time, Tcycle.

Chip-level approach

The chip level SER contributions due to clock upsets (jitter and race) are computed by using the pulse width at every node of the clock network and the corresponding timing derating. As discussed in [3], the derated SER ($SER_{derated}$) equals the product of TD and the nominal SER ($SER_{nominal}$). $SER_{nominal}$ of a node here is defined as the SER at the minimum Qcrit required to produce the required pulse width $Wcrit^n$ at clock node n. $SER_{nominal}$ of clock node n is then computed using SPICE simulations. This is a fast and simple SER simulation that involves only 1 gate. Charge is injected into the node of interest and the output of the gate is monitored. The amount of charge that results in the formation of a pulse wider or equal to $Wcrit^n$ is then used to compute the relevant SER. If the gate along the clock path has several inputs, the worst case SER of all input vector combinations is used. This process is repeated until all the clock paths have been covered. Finally, $SER_{derated}$ is computed from $SER_{nominal}$ and TD of every node of the clock path for all the paths. If a node is connected to multiple paths then the maximum SER of all paths is applied in the analysis.

Figure 5 shows the comparison between accurate SPICE based results (TIDEST) and our quasi-analytical approach for different data arrival times, or more accurately margins. Margin/Tcycle in Figure 5 denotes the data timing margin as a fraction of the cycle time. One can see that in the clock jitter domain the accuracy of the analytical model is very poor and not conservative. However, in the race dominated timing regime, the analytical model consistently gives conservative results within about 2x of our TIDEST results. The inaccuracy is the result of modeling the Wcrit as full rail pulses only. This is a good assumption if a new clock edge (rail to rail) needs to be generated, but a poor approximation in cases where the clock edge needs to be only slightly moved. However, we will see in the next section that the high inaccuracy in the jitter regime turns out to be irrelevant for the accuracy of the chip-level assessment.

Please note that a relative margin of "1" in Figure 5 is not very realistic since it corresponds to data arriving at the receiving sequential right after it has been released from the previous sequential in a pipeline. This would be approximately valid for very short data paths and very long cycle times.

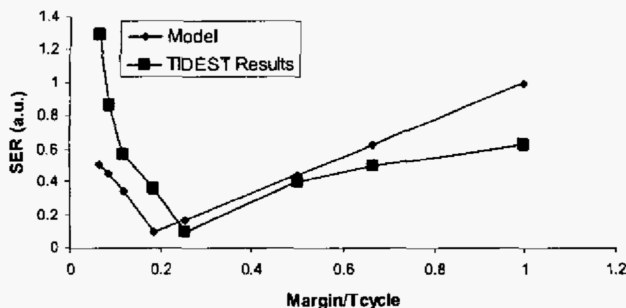

FIGURE 5. COMPARISON BETWEEN TIDEST RESULTS AND OUR ANALYTICAL MODEL AS A FUNCTION OF DATA ARRIVAL TIME (MARGIN)

An interesting outcome of our study is shown in Figure 6, where a typical trend of the SER due to clock node hits is plotted as a function of distance from the receiver. Clearly, the contribution due to clock node hits decreases with distance from the receiver. The exact shape, however, critically depends on the node capacitances as well as the glitch propagation behavior as accounted for in Wcrit. For instance, upsets occurring in clock registers break the trend observed in Figure 6. The main reason for this is the fact that upsets occurring in the registers yield (false) data as opposed to glitches and are not subject to attenuation.

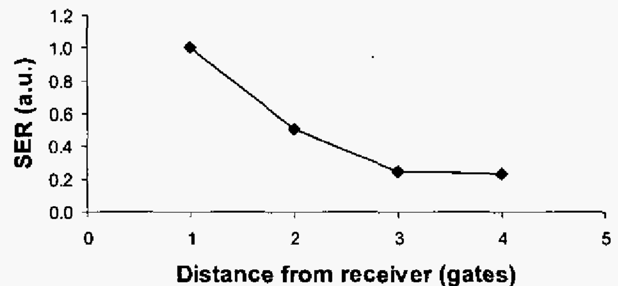

FIGURE 6. SER DUE TO CLOCK NODE UPSETS AS A FUNCTION OF DISTANCE TO THE RECEIVER

RESULTS and DISCUSSION

All results presented here are based on the simulation methodology introduced in the previous section. The evaluated designs are test cases designed in a state of the art process technology.

High-Level Schematics of Sequentials

Schematics of the non-hardened Master/Slave FF (M/S FF), pulse latch (PL) and pulse generator (PG) designs are depicted in Figure 7. In order to allow for a fair comparison of the failure rates of the pulse latch and the M/S FF, sequentials with comparable output drive strengths have been selected. The investigated sequentials have not been optimized for SER prior to this study. All SER results presented in this study are based on layout extracted netlists.

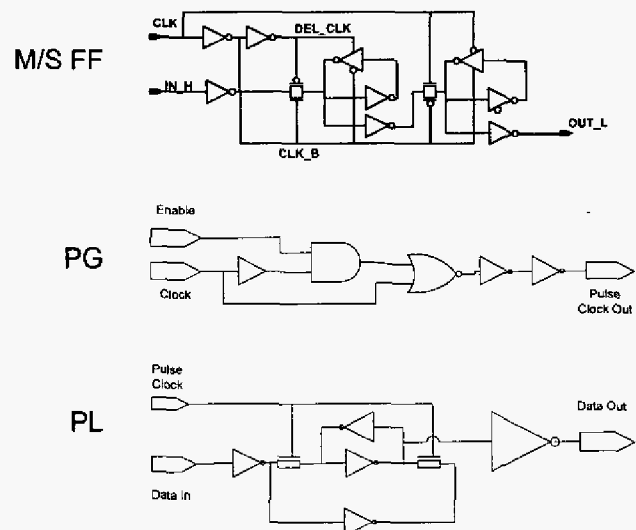

FIGURE 7. SCHEMATICS OF THE NON-HARDENED SEQUENTIALS

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External Clock Node Contribution

We have simulated the SER contribution due to clock nodes along the clock distribution path using the modeling methodology described in the previous section. Our results prove that upsets along the section of the clock path before the clock grid are absolutely negligible for the designs studied. The main reasons for this trend are 1) the large node capacitances and consequently large Qcrit values of global clock nodes, 2) the small total cross section of the charge collection area of the global clock network as compared to that of the local nodes at the clocked receivers, and 3) the RC filtering capabilities of the clock grid itself. The total contribution of the global clock network is estimated to be less than 0.1% of the overall clock path SER, which is dominated by contributions from local but external clock buffers and clock buffers that are internal to the receivers.

Local Clock Node Contribution

Local here denotes internal nodes as well as external clock nodes that are located after the regional clock grid. Both contributors show a very similar SER trend as a function of margin with respect to the latching edge of the receiver. This is not surprising since the definition of internal and external is purely arbitrary and artificial. Figure 8 plots and compares the SER values for external but local (solid squares) and internal clock nodes (dashed line) for a FF based design. One can clearly see the steep increase due to radiation-induced clock jitter. The main reason for this steep increase is that the less margin data have, the less the clock edge needs to be moved to induce a fault. The minimum critical charge (triangles) correlates strongly with the amount the clock edge needs to be moved and decreases steeply with decreasing margins. Surprisingly, Qcrit exhibits a maximum. This maximum denotes the onset of a different clock node related upset mode, radiation-induced race. In the transition region, a lot of charge is needed to move the clock edge sufficiently far to result in an upset. Further, generation of a new clock edge is not likely in this region to result in a latched fault, mainly because data arrive too late in order to be able to propagate into the latching element. In the transition region a wider pulse width is needed to give the data sufficient time to overwrite the old value in the sequential. In the race dominated regime the SER increases almost linearly. This reflects the fact that the critical charge to generate new clock edges is fairly constant and the increase in SER is mainly due to an increasing TD with increasing data timing margins.

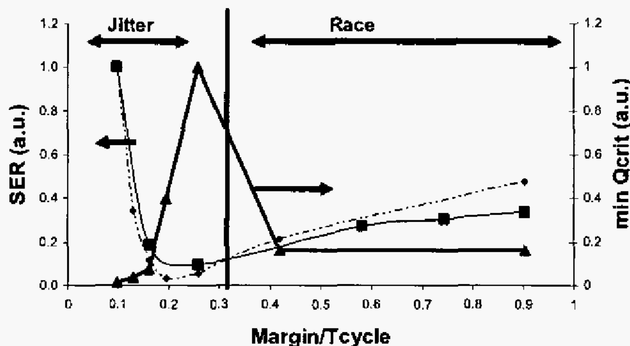

FIGURE 8. CLOCK NODE-SER AND QCRIT AS A FUNCTION OF DATA MARGIN FOR A FF BASED DESIGN

Since the SER data in Figure 8 need to be integrated over the critical path delay distribution, the steep increase in SER at small margins has little impact on the overall chip-level SER. For the FF based design studied, the contribution due to jitter is less then 2% of the total clock path SER. This explains why errors in our modeling in this regime have little impact on the accuracy of our overall results.

Due to the fact that the SER of clock node upsets decreases with increasing distance from the receiver (see Figure 6), and accounting for the average number of external but local clock nodes per sequential, external clock nodes contribute in average less than 20% of the total clock path SER for FF based designs. The number is even lower for pulse latch based designs. Our study clearly shows that only the first two or three clock nodes, whether internal or external, need to be accounted for in the overall clock network SER budget.

Please note that the SER of M/S FFs as a function data arrival time (or equivalently clock speed) has been published and discussed in detail in [3, 4] and is not repeated here. In [3] it is shown that for M/S FF based designs the SER of M/S FF is expected to linearly decrease with increasing clock speed.

In Figure 9 the trend in clock path SER is plotted for a pulse latch (PL) based design, i.e. for a pulse generator (PG). In such a design, a local clock pulse is generated that is fed into pulse latches. Typically these pulses have widths in the tens of ps. Any distortion of such a fragile entity can result in data incorrectly being latched by the receiving pulse latch. Similar to FF based designs, a steep increase due to jitter is observed. At small margins data just arrive in time to be latched and any radiation-induced jitter might result in a fault, similarly to M/S FFs. The SER trend shows again a local minimum. After the local minimum, the SER increases monotonically in the whole investigated data time-margin range due to an increasing TD. This hints that the minimum in clock SER as a function of margin is a universal observation, valid for very different types of sequentials.

In the case of pulse generators, a pulse that is wide enough to allow data being written into the pulse latch needs to be generated in the race regime. Usually this minimum pulse width is not very different from M/S FFs, which explains the similarity of the SER trends for both types of devices.

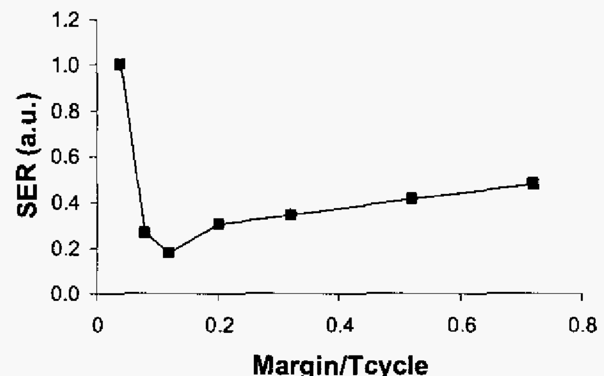

FIGURE 9. CLOCK-SER AS A FUNCTION OF DATA ARRTIVAL TIME (MARGIN) FOR A PULSE LATCH BASED DESIGN

We would like to emphasize that classical race (min-delay) can in principle be induced by radiation. For instance, if the pulse is distorted such that data are sampled later in time at the receiving sequential (shifted pulse), race could occur for sufficient skew between two sequentials along a data path. However, as explained previously, in our study skew between sequentials has been set to

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zero and the data paths studied have sufficient margins so that radiation-induced skew was highly unlikely. Since min-delay violations result in functional problems that cannot be fixed by reducing the clock speed, designers are investing considerable time in making sure that skew is small and data paths have sufficient margin in all process corners. Further, the simulation setup used for deriving the data plotted in Figures 8 and 9 comprise of only one sequential element and min delay problems (classical race) therefore is impossible here. We do not believe that this resulted in a large error in our chip-level SER assessments. Similarly to clock-induced jitter, where the corresponding chip-level SER contribution is vanishingly small because the relative number of critical paths is very small, the contribution of radiation-induced min-delay is believed to be negligible too.

We have investigated radiation-induced jitter and race of sequentials as a function of clock speed built in the same technology. In this case a simulation setup similarly to the one shown in [3, 4] has been used, where the data path comprises of a few inverters embedded between two sequentials. Solely clock nodes that feed into the downstream sequential have been upset (without loss of generality [3]). Figure 10 depicts the ratio of clock path SER versus sequential SER for an M/S FF. Please note that the results are only valid for one particular data path length. Fmax here denotes the maximum possible clock speed that the investigated data path allows. According to these results, radiation-induced jitter, not corrected for actual data arrival times, can contribute more than 100% of the derated non-clock FF SER. Once realistic delay distributions have been factored in, the gross of the FF clock path SER is due to race as discussed above.

For the investigated FF based design, the *average integrated* clock SER, which is dominated by radiation-induced race, is about 5% of the *nominal* non-clock FF SER at the investigated conditions, or about 20% of the derated average FF SER [3].

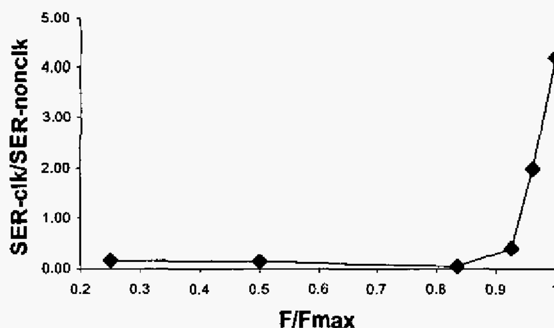

FIGURE 10. THE RATIO OF CLOCK-SER TO NON-CLOCK-SER OF MASTER-SLAVE FFS INCREASES EXPONENTIALLY WITH CLOCK SPEED FOR CRITICAL PATHS (I.E., HIGH F/FMAX).

Figure 11 plots simulation results for a non-hardened pulse latch and non-hardened pulse generator compared to the total M/S FF-SER as a function of clock speed. As in the case of Figure 10, the delay distribution has not been factored in. What we learn from Figure 11 is that the pulse generator studied exhibits the highest SER in a large frequency range for the studied data path example. In the case of critical paths (i.e. at the maximum clock speed) the SER contribution due to jitter is orders of magnitude larger than the *derated* sequential SER that does not include clock node upsets. Please note that for the data shown in Figure 11 it is assumed that the each pulse generator feeds one pulse latch (a not very realistic case).

At first sight one might expect that the pulse latch has a considerably lower SER than the M/S FF, since the M/S FF has two state elements, whereas the pulse latch has only one. However, the window of vulnerability or timing derating is about twice as long for the pulse latch. For the M/S FF, the slave and the master latch are each vulnerable for about 50% of the cycle (at slow clock speeds), whereas the pulse latch is susceptible for about 90% of the time (Figure 12). This compensates for the smaller area cross section of the pulse latch.

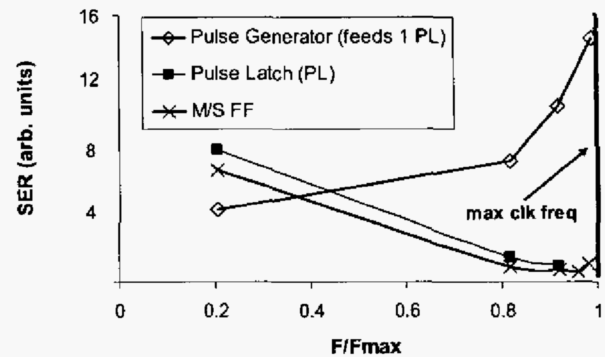

FIGURE 11. CLOCK FREQUENCY DEPENDENCE OF RADIATION-INDUCED CLOCK NODE SER

For unhardened devices, pulse generator nodes exhibit critical charges that are up to 10x lower than those of unhardened pulse latch nodes (Figure 11). Due to the high susceptibility of the clock generator nodes, the unhardened version is susceptible even to alpha-particle induced upsets (see Table 2 and Figure 12).

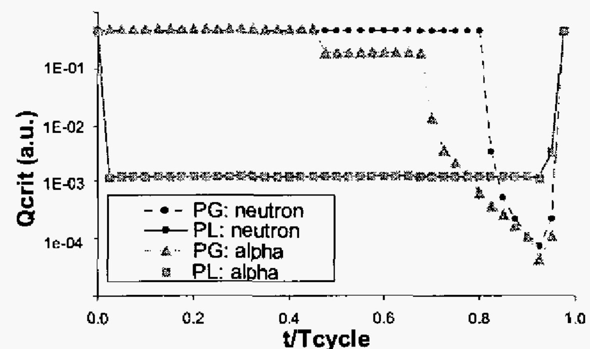

FIGURE 12. QCRIT SIMULATION RESULTS FOR ONE PULSE GENERATOR NODE AND ONE PULSE LATCH STATE NODE

Figures 11 and 12 further underline the high susceptibility of the pulse generator to SEU. Figure 12 compares the critical charges of a pulse latch state node and of one clock node in the pulse generator as a function of time when the particle hit occurs within one cycle. Unhardened pulse generator nodes are clearly more susceptible to upsets by both neutrons and alpha particles than the unhardened pulse latch state nodes. The slight difference in shape in neutron and alpha-particle Qcrit for the selected PG node in Figure 12 is due to the corresponding differences in charge collection waveforms for neutrons and alpha-particles.

The steep increase at high clock frequencies –or critical paths- occurs due to radiation-induced clock jitter, equivalently to Figure 9. Similarly to the clock frequency trends observed for M/S FFs, the failure rate of the pulse latch decreases with increasing clock

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frequency. This is not surprising given the fact that pulse latches behave similar to M/S FFs. Both types of sequentials are essentially edge triggered. Please recall that the decrease in SER is a direct consequence of the decreasing timing derating [3]. This is because any upset in the sequential has to propagate in time to the next downstream sequential in order to be of relevance. It is worth mentioning that the M/S FF SER in Figure 11 accounts for jitter and race. Therefore, at very high clock speeds the SER of the M/S FF increases due to radiation-induced clock jitter as explained in [3].

For the investigated non-hardened pulse latch based design, the *average integrated* SER due to jitter and race equals up to 90% of the *derated* pulse latch SER at the investigated conditions.

Hardening Techniques

Our simulation data provide strong evidence that radiation-induced clock jitter and race dominate the SER of high-speed data paths for pulse latch based designs and necessitates adequate mitigation techniques for high RAS products. We have learned in the previous sections that the final contribution due to clock node upsets is of the order of 20% of the total sequential SER for M/S FF based designs. It is even of the order of 90% for pulse latch based designs under the investigated conditions (i.e., non shared case). Therefore, neglecting the impact of jitter and race can result in significant errors in the chip-level SER assessment. Clearly, the previous sections have proven that the contributions due to clock node upsets cannot be neglected.

After the importance of upsets in the clock tree has been recognized, adequate mitigation techniques need to be developed to limit this contributor. In this study we present results of our mitigation efforts for pulse latch based designs. In the case of FF based designs the ROI of hardening clock paths is much smaller and therefore not discussed here. Nevertheless, even for FF based design, clock node upsets needs to be accounted for in the SER assessments.

We have designed hardened pulse generators and pulse latches to lower the SER contribution due to upsets along the clock path. In the case of the pulse generator, node engineering was performed to minimize the charge collection area and replace the lost capacitance with gate capacitance (i.e., "good capacitance) [6]) by adding dummy transistors to the internal clock generator clock nodes. This lowered the susceptibility of the pulse generator by about 3x. The SER due to clock node upsets in the pulse generator (PG) was further reduced by sharing the pulse generator between several pulse latches. Sharing the pulse generator with as many pulse latches as possible proves to be an efficient way to reduce the SER in pulse latch designs. If the pulse generator is shared with 10 or more pulse latches, the SER contribution due to pulse generator hits becomes sufficiently small. Sharing a) reduces the cross section for charge collection and b) increases the capacitance on some of the internal clock nodes. Sharing the PG with significantly more pulse latches is not feasible due to minimum delay problems caused by RC related skew.

The hardened pulse latch design uses an interlocked redundant state node scheme that duplicates the state information similar to the DICE design [7]. A Muller C-element at the output guarantees that information is propagated only if both state copies agree. The design further was optimized by node engineering methods as described in [6]. The SER of the hardened pulse latch is more than a factor of 20 lower than that of the non-hardened design.

The discussed hardening measures result in an increase in area and power, but it turns out that the hardened pulse generator and pulse latch consumes still less power and has a smaller footprint than the reference M/S FF design (table 1). Without sufficient sharing or additional hardening the pulse latch design is inferior to the M/S FF based design in terms of SER for high-speed applications.

TABLE 1. RELATIVE SEQUENTIAL PERFORMANCE VALUES

Cell	Area	# Of Gate Delays
M/S	1.0	3
PL	0.7	1.5
SERhard PL	1.05	2.5

An alternative hardening technique is presented in [8], where the authors introduce a circuit design technique based on an isolated well process technology that seems suitable for mitigating single event transients along the clock path.

Table 2 summarizes the simulation results of the hardened and unhardened elements at the product's respective target operating conditions and compares it to the reference M/S FF design. The results are valid for the investigated data path topology and are not necessarily representative of the chip-level results. The unhardened pulse latch shows a 33% higher failure rate than the M/S FF, if hits in the clock generator are not taken into account. For a pulse latch based design with unshared pulse generators, the pulse generator increases this number by another 50%. Although the hardened pulse latch based design is only 5% larger in area than the M/S design, it is still faster and significantly more robust with respect to radiation-induced upsets than the unhardened designs (table 1). For the investigated data path, the hardening techniques discussed above yield a ~23x reduction in overall sequential SER (including clock node upsets).

TABLE 2. HIGH LEVEL SUMMARY OF ALL SIMULATION RESULTS FOR ONE DATA PATH

Device	alpha - SER %	neutron - SER %	relative SER
M/S FF	14.80	85.20	1.00
pulse latch	7.97	92.03	1.33
pulse generator	32.35	67.65	0.51
pulse latch + pulse generator (driving 10 pulse latches)	8.86	91.14	1.38
hardened pulse latch + pulse generator (10 pulse latches)	11.71	88.29	0.06

Chip-Level SER

In the previous sub-section we discussed radiation-induced failure rates of clock path nodes and clock devices relative to the failure rates of the receivers. We presented the different SER trends as a function of data arrival times, clock speed and device types. Here we will show how this relates to the big picture and present the results of our chip-level SER assessments for the two studied designs: one using M/S FFs and one using pulse latches.

The chip-level SER has been assessed similarly to the methodology described by Nguyen et al [9]. Table 3 summarizes the relative radiation-induced jitter contributions of the investigated designs as a percentage of the total estimated SER. For the investigated FF based design the clock SER is estimated to contribute about 9% of the total SER, whereas for the unhardened and unshared PL design it equals about 52% (i.e., 1 PG per pulse latch). In this case, hardening or some other SER mitigation

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technique for protecting sequentials is highly desirable. The simple clock generator hardening techniques discussed in this paper reduce the clock SER contribution to virtually nothing. This assumes that all pulse generators are hardened on the chip and each pulse generator feeds 10 pulse latches. Finally, the hardened pulse latch design (i.e., PG and PL hardened) is estimated to have the lowest total chip-level SER at about 65% of the SER of the studied FF based design.

We have not investigated the scaling trend of radiation-induced clock SER in this work. However, we would like to mention that clock SER depends on glitch attenuation and propagation along the clock path, analogous to glitch propagation in static logic along a data path. We therefore expect that radiation-induced static logic failure rates and clock SER scale very similarly.

TABLE 3. CONTRIBUTION OF CLOCK SER IN % RELATIVE TO THE TOTAL CHIP-LEVEL SER

	FF design	PL design	hardPG/unhardPL	hardPL/hardPG
Clock SER	9	52	1	0

SUMMARY

We have investigated the impact of radiation-induced clock jitter and race on the chip-level SER for two different design styles. The evaluated designs are test cases designed in a state of the art process technology. To assess the chip-level impact of upsets along the clock path, we developed a novel methodology that accounts for radiation-induced glitch generation and propagation in the clock network. This methodology enabled us to efficiently estimate the SER of clock nodes. Upsets induced in clock synthesizing global clock generators (PLLs) have not been taken into account in our SER assessment. We believe that this simplification results in a small error in our SER assessment. This is mainly due to the small area cross section of the PLL and the glitch filtering capabilities of the RC component of the PLL.

Our key findings are:

1) The radiation-induced failure rate contribution of the global clock network is negligible. The majority of radiation-induced jitter is due to upsets of local clock nodes. Only the first 3-4 clock nodes (counted from the receiving sequentials) contribute significantly to the overall clock SER.

2) Clock SER shows two distinct modes of upsets: a) radiation-induced jitter and b) radiation induced race. Race here is due to the radiation-induced generation of a new clock edge or clock pulse.

3) Due to the small number of critical paths, radiation-induced jitter contribute less than 1% of the total clock SER

4) In the case of FF based designs, radiation-induced race accounts for about 20% of the average derated FF SER at the investigated conditions.

5) Pulse generators are very susceptible if not protected by hardening measures. In our unhardened example radiation-induced race in case of the pulse generator accounted for up to 90% of the average derated pulse latch SER.

6) Mitigation techniques presented for pulse latch based designs yielded significantly reduced pulse latch SER and pulse generator SER values. Our simulations project a 20x reduction in SER for the hardened pulse latch and a 3x reduction for the hardened pulse generator. Sharing of the pulse generator is the most effective means to reduce the clock SER of pulse latch based designs.

7) Clock SER cannot be neglected and can potentially add a significant adder to the chip-level SER. In the case of the studied FF based design, the radiation-induced clock failure rate accounted for about 10% of the overall chip-level SER, in the case of the unhardened pulse latch design, the it reached 50%.

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